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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,183	03/17/2004	Chiou-Feng Chen	A-75030	5108

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EXAMINER	
NGUYEN, HIEN N	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,183	CHEN ET AL.	
	Examiner	Art Unit	
	Hien N. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *the Election/Response filed on 5/18/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *31 and 32* is/are withdrawn from consideration.

5)☒ Claim(s) *1-13,18,21 and 22* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *14-17, 19-20, 23-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search Report*.

DETAILED ACTION

1. The Election/Response filed on 5/18/05 for NOT canceling the non-elected claims (Group II) is found non-responsive (MPEP § 821.03). Therefore, **claims 31-32 are withdrawn** from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group II, there being no allowable generic or linking claim. Election was assumed **without** traverse in the reply filed on 5/18/05.

2. Claims 1-30 are presented for examining.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-12, 13, 18 and 21-22 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No. **10/802,253 (**herein after **Reference)**. Although the conflicting claims are not identical, they are not patentably distinct from each other because the type of connection such as NAND structure in a flash memory

(as recited in claims 1, 13 and 18 of the present application) in the preamble is obviously a matter of design choice in which individual cells can be connected in series or parallel. More specifically, a list of matching claims between the instant application and the **Reference** is as follow:

Instant application	Reference
1	**1, 13**
2	**3**
3	**4**
4	**2**
5	**5**
6	**6**
7	**7**
9	**8**
10	**9**
11	**10**
13, 18	**13**
21	**14**
22	**8**

3. For instance, as for **independent claim 1**, an argument of inherency exists as follows: "the bit line diffusion and the source region" as recited in claim 1 is actually "the common source region" as recited in claim 1 of the Reference. Furthermore, even though claim 1 of the instant application has not specifically recited that "the floating gates and the control gates" are arranged above the active area, it is known in the art of Flash memory that the gates (floating and control gates) must be above "the source region" (i.e. the active area).

Application 10/803183
1. A NAND flash memory cell array, comprising: a substrate having an active area, a bit line diffusion and a source region spaced apart from each other toward opposite sides of the active area, a plurality of vertically stacked pairs of floating gates and control gates **arranged in a row between the bit line diffusion and the source region**, with the control gates being positioned above and aligned with the floating gates, a select gate and an erase gates aligned with and positioned on opposite sides of each of the stacked gates, with select gates at the ends of the row partially overlapping the bit line diffusion and the source region, a diffusion region in the active area beneath each of the erase gates, a bit line above the row, and a bit line contact interconnecting the bit line and the bit line diffusion.

Application 10/802,253
1. A flash memory cell array, comprising: a substrate having an active area, a plurality of vertically stacked pairs of floating gates and control gates arranged in rows **above the active area**, with the control gates being positioned above and aligned with the floating gates, select and erase gates aligned with and positioned on opposite sides of each of the stacked gates, a bit line above each row, bit line diffusions in the active area between and partially overlapped by two select gates, **a bit line contact interconnecting the bit line and the bit line diffusions in each row, and a common source region in the active area beneath** the erase gate and partially overlapped by the floating gates.

4. As for claim 2, the recitation of "*the control gates, the select gates and the erase gates surround the floating gates in a manner which provides a relatively large inter-gate capacitance for high-voltage coupling during an erase operation*" is encompassed with the recitation of "*the control gates, select gates and erase gates surround the floating gates in a manner which provides a relatively large inter-gate capacitance for high-voltage coupling during an erase operation*"(claim 3 of Reference)

5. Another example: as for claim 4, the recitation of "a relatively thin tunnel oxide

between the floating gates and the substrate, and relatively thick dielectrics between the floating gates and *the other gates*" is encompassed with the recitation of "a relatively thin tunnel oxide between the floating gates and the substrate, **a first** relatively thick dielectric between the floating gates and the select and erase gates, and a **second** relatively thick dielectric between floating gates and control gates" since "other gates" are "select and control gates".

Other remaining claims are rejected with the obviousness and inherency as shown in the examples above since the claims of this instant application are more specific than the broader claims of the Reference.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Allowable Subject Matter

6. Claims 14-15, 19-20 and 23-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The primary reason for allowance is for at least the reason of different programming voltages applied to a cell are not suggested in the art of references as disclosed specifically in claims 14-15, 19-20 and 23-30.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Van Houdt (6,486,509), Hsieh (6,818,512) and Guterman et al.(6,861,700) disclose a split-gate flash memory and are cited as of interest.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hien N. Nguyen whose telephone number is (571) 272-1879. The examiner can normally be reached on Monday through Thursday 9:30 AM to 7:00 PM..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

H. Nguyen HN
August 18, 2005

Hien Nguyen
Patent Examiner